AMENDMENTS TO THE CLAIMS

1. (Currently amended) A method for generating a UWB signal comprising the step of differentiating a clock signal once to obtain the UWB signal wherein the step of differentiating the clock signal comprises feeding the clock signal to an input of an amplifier and negatively feeding back an output of the amplifier, through a low pass filter, to the amplifier input.

2. (Original) A method according to claim 1 further comprising the step of differentiating the UWB signal at least once to generate a monocyclical or a polycyclical UWB signal.

3. (Original) A method according to claim 1 further comprising the step of modulating a data signal with the UWB signal to obtain a modulated UWB signal.

4. (Original) A method according to claim 3 further comprising the step of differentiating the modulated UWB signal at least once to generate a monocyclical or a polycyclical UWB signal.

5. (Original) The method of claim 3 wherein the modulated UWB signal is amplitude-modulated.

6. (Original) The method of claim 3 wherein the modulated UWB signal is pulse-position-modulated.

7. (Original) A method for generating a UWB signal in a system comprising:

an amplifier having an input and an output;

negative feedback means;

a low-pass filtering means; and

a DC decoupling means

wherein the method comprises:

providing an output of the system to the low-pass filtering means to produce a low-pass filtered output;

feeding back, by the negative feedback means, the amplifier low-pass filtered output to the input of the amplifier;

applying the DC decoupling means to remove DC components from the amplifier output; wherein

the output of the system is an amplified differential of an input signal to the system; and

whereby a UWB pulse is produced for transmission.

8. (Original) A method according to claim 7 wherein the amplifier means comprises a biased transistor.

9. (Currently amended) A method as claimed in claim 7 ~~claim 7 or 8~~ wherein the input signal is a clock signal.

10. (Currently amended) A method as claimed in claim 7 ~~claim 7 or 8~~ wherein the input signal is a saw tooth signal.

11. (Currently amended) A method as claimed in claim 7 ~~claim 7 or 8~~ wherein the input signal is a pulse signal.

12. (Currently amended) A method as claimed in claim 7 ~~claim 7 or 8~~ wherein the system is implemented in an Integrated Circuit.

13. (Currently amended) A method as claimed in claim 7 ~~claims 7 to 12~~ wherein the system comprises current-voltage topology.

14. (Currently amended) A method as claimed in claim 7 ~~claims 7 to 12~~ wherein the system comprises voltage-voltage topology.

15. (Currently amended) A method as claimed in claim 7 ~~claims 7 to 12~~ wherein the system comprises voltage-current topology.

16. (Currently amended) A method as claimed in claim 7 ~~claims 7 to 12~~ wherein the system comprises current-current topology.

17. (New) A system comprising:

an amplifier having an input and an output;

negative feedback means;

a low-pass filtering means;

DC decoupling means;

the amplifier providing an output of the system to the low-pass filtering means to produce a low-pass filtered output;

the negative feedback means feeding back the low-pass filtered output of the amplifier is negatively fed back to the input means of the amplifier;

the DC decoupling means removing DC components from the amplifier output; wherein

the output of the system is an amplified differential of an input signal to the system; and

whereby

a UWB pulse is produced for transmission.

18. (New) A system as claimed in claim 17 wherein the amplifier means comprises of a biased transistor.

19. (New) A system as claimed in claim 17 wherein the input signal is a clock signal.

20. (New) A system as claimed in claim 17 wherein the input signal is a saw tooth signal.

21. (New) A system as claimed in claim 17 wherein the input signal is a pulse signal.

22. (New) A system as claimed in claim 17 wherein the system is implemented in an Integrated Circuit.

23. (New) A system as claimed in claim 17 wherein the system comprises current-voltage topology.

24. (New) A system as claimed in claim 17 wherein the system comprises voltage-voltage topology.

25. (New) A system as claimed in claim 17 wherein the system comprises voltage-current topology.

26. (New) A system as claimed in claim 17 wherein the system comprises current-current topology.